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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,565	09/12/2003	Howard Rhodes	M4065.0570/P570-A	5308
24998	7590	03/22/2006	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP 2101 L Street, NW Washington, DC 20037				ARENA, ANDREW OWENS
ART UNIT		PAPER NUMBER		
		2811		

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

BV

Office Action Summary	Application No.	Applicant(s)
	10/660,565	RHODES ET AL.
	Examiner	Art Unit
	Andrew O. Arena	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 January 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 90 and 93-141 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 90 and 93-141 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 10 January 2006 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>01/10/2006</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 124 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
3. Regarding claim 124, it seems that forming the capacitor over the active area of the photosensor would block light from reaching the photosensitive area, rendering the invention inoperable. If the invention could function with the structure claimed in claim 124, applicant must describe how this is possible.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 90, 93-107, and 130-136 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 90 and 130 fail to correspond in scope with that which applicants regard as the invention can be found in the drawings (Fig 10) and the specification ([0008] ln 4, [0036] ln 9). This figure indicates that the invention is different

from what is defined in the claims because it clearly depicts the charge storage capacitor does not "overly exclusively said field oxide region" but also overlies insulating layer 117, doped region 120, and substrate 116. For art-based rejection purposes, the cited limitation will be interpreted to read on any charge storage capacitor that overlies any field oxide region.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 90-141 are rejected under 35 U.S.C. 102(b) as being anticipated by Rhodes (US 6,204,524).

8. Regarding claim 90, Rhodes discloses (Fig 6-14) a method of forming a CMOS imager (col 8 ln 28-30) comprising the steps of:

providing a semiconductor substrate (116+120; col 8 ln 30-32) having a doped layer (120) of a first conductivity type (col 8 ln 32-33);
forming a first doped region (155; col 7 ln 61) of a second conductivity type (col 7 ln 30-32) in said doped layer, said first doped region being adjacent a field oxide region (115; col 7 ln 25-27);

forming a charge storage capacitor (col 7 ln 65) such that the entire extent of said charge storage capacitor overlies [exclusively] said field oxide region (no extent of 162 lies under 115); and

forming a direct contact (150) between said first doped region and said charge storage capacitor (Fig 5: 150; col 7 ln 61-64, col 8 ln 11-13; forming: col 9 ln 36-50).

9. Regarding claim 93, Rhodes discloses (Fig 10-14) said charge storage capacitor (162) is formed by:

forming a first conductive layer (156; col 9 ln 49-51) over said substrate (col 7 ln 66-67, col 9 ln 28-30, 49-52) including said field oxide region (apparent in Fig 5, 10-14);

forming a dielectric layer (158) over said first conductive layer (col 9 ln 67); and

forming a second conductive layer (160) over said dielectric layer (col 10 ln 14).

10. Regarding claim 94, Rhodes discloses said first and second conductive layers are independently selected (col 10 ln 15-17) from doped polysilicon (col 10 ln 17-18).

11. Regarding claim 104, Rhodes discloses (Fig 8, col 9 ln 8-9, 15-16):

forming a second doped region (126) of said second conductivity type in the doped layer spaced from said first doped region (110) to transfer charge (col 9 ln 9-10, col 7 ln 35-37) from a charge collection area (125+162);

forming a third doped region (130) of said second conductivity type in the doped layer spaced from said second doped region wherein said third doped region effectuates the transfer of charge to a readout circuit (col 9 ln 10-12, col 7 ln 44-50); and

forming a fourth doped region (134) of said second conductivity type in the doped layer spaced from said third doped region wherein said fourth doped region is a drain for a reset transistor (col 9 ln 12-13, col 7 ln 55-56) for said CMOS imager.

12. Regarding claim 105, Rhodes discloses said first conductivity type is p-type (col 7 ln 23-35, col 8 ln 32-34) and said second conductivity type is n-type (col 7 ln 32-33).

13. Regarding claim 106, Rhodes discloses (Fig 8) forming a photogate (102; col 8 ln 46) over said doped layer between said first (155) and second (126) doped regions.

14. Regarding claim 107, Rhodes discloses (Fig 5) connecting an electrode (156) of said storage capacitor to said photogate (156 connects to 102 via 155, 110, and 100; col 8 ln 10-14).

15. Regarding claim 122, Rhodes discloses (Fig 6-14) a method of forming an imager (col 8 ln 28-30) comprising the steps of:

providing a semiconductor substrate (116+120; col 8 ln 30-32) having a doped layer (120) of a first conductivity type (col 8 ln 32-33);

forming a field oxide region (115; col 7 ln 25-28) in said semiconductor substrate;

forming a photosensor (125; col 7 ln 36-37. Formed: col 8 ln 45 – col 9 ln 25) including a charge collection region (110) of a second conductivity type (col 7 ln 31-32), said charge collection region being provided in said doped layer (col 7 ln 30-31);

forming a floating diffusion region (155; floating - not connected to fixed potential) for receiving charge from said charge collection region (col 7 ln 61-64); and

forming a charge storage capacitor (162; col 9 ln 36-37) over said semiconductor substrate (col 7 ln 66-67) so that one electrode (156) of said storage capacitor is

connected directly to said floating diffusion region by an electrical contact (150; col 8 ln 10-13).

16. Regarding claim 123, Rhodes discloses (Fig 5) the entire extent of said charge storage capacitor overlies said field oxide region (no portion of 162 lies under 115).

17. Regarding claim 124, Rhodes discloses (Fig 5) the entire extent of said charge storage capacitor overlies an active area of said photosensor (no portion of 162 lies under 125).

18. Regarding claim 125, Rhodes discloses (Fig 5) said charge storage capacitor is formed partially (col 8 ln 20-21) over said field oxide region (left side of 162) and partially over an active area of said photosensor (right side of 162).

19. Regarding claim 126, Rhodes discloses (Fig 14) the other electrode (160) of said charge storage capacitor is connected to ground (col 10 ln 25-28).

20. Regarding claim 127, Rhodes discloses (Fig 5) the other electrode of said charge storage capacitor is connected to a gate of a transistor (there exists a connection pathway from 160 to 108 of 128).

21. Regarding claim 128, Rhodes discloses (Fig 14) said transistor (ex, 128) is part of a three-transistor cell (ex. 102, 128, 132).

22. Regarding claim 129, Rhodes discloses (Fig 5) said transistor (ex, 128) is part of a four-transistor cell (ex. 102, 128, 132, 136).

23. Claims 130-136 are rejected under 35 U.S.C. 102(b) as being anticipated by Han et al. (US 2001/0006238) – hereinafter Han.

24. Regarding claim 130, Han discloses (Fig 4A-4E) a method of forming an imager [0026] comprising the steps of:

providing a semiconductor substrate (202; [0027] ln 1-2) having a doped layer (epitaxial layer of [0027] ln 14-17) of a first conductivity type (p-type);
forming a field oxide region (208) in said semiconductor substrate ([0027] ln 1-4);
forming a photodiode (212) in said doped layer ([0023] ln 5-9);
forming a charge storage capacitor (230; [0025] ln 1, [0028]-[0031]) such that the entire extent of said charge storage capacitor overlies [exclusively] said field oxide region (no extent of 230 lies under 208); and

connecting an electrode of a charge storage capacitor directly to said photodiode by an electrical contact (235; which clearly contacts 212 in Fig 4E).

25. Regarding claim 131, Han does not limit his connection to any particular connection type, therefore, the disclosure encompasses all well-known connection types, including connecting an electrode of said storage capacitor to ground.

26. Regarding claim 132, Han discloses (Fig 4E) the other electrode of said charge storage capacitor is connected to a gate of a transistor (there exists a connection pathway from 235 to 207 of 210).

27. Regarding claim 133, Han discloses said transistor is a transfer transistor (210; [0027] ln 4).

28. Regarding claim 134, Han does not limit his transistor to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor types, including a source follower transistor.

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29. Regarding claim 135, Han does not limit his transistor to any particular type ([0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor types, including a row select transistor.

30. Regarding claim 136, Han discloses said transistor is part of a three-transistor cell (ex. transfer, reset, and amplification : [0024] ln 11-13, 16-19).

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

32. Claims 95-103, 108-121, and 130-136 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes in view of Han.

33. Regarding claim 95, Rhodes discloses the method of claim 90, but does not disclose "forming an element of said CMOS imager simultaneously with forming said storage capacitor." Han discloses an analogous CMOS imager [0002] and teaches the method of the current claim ([0015], Fig 4A-4E: [0026] – 0031]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Rhodes by forming the planar capacitor on the same level as the transistor gate, as taught by Han, using the manufacturing method taught by Han; for at least the purpose of reducing the steps of manufacture (Han: [0032]).

34. Regarding claim 96, Rhodes as modified by Han discloses said element is a transistor gate (Han: [0015], Fig 4A-4E: 207, [0026] – 0031]).
35. Regarding claim 97, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said transistor gate (there exists a connection pathway between 235 and 207).
36. Regarding claim 98, Rhodes as modified by Han discloses (Han: Fig 4E) said element is a transfer gate (207; [0024] ln 11-12).
37. Regarding claim 99, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said transfer gate (a connection path exists between 235 and 207).
38. Regarding claim 100, Rhodes as modified by Han allows for plural transistors, and does not limit the transistors to any particular type (Han: [0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a source follower gate.
39. Regarding claim 101, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said source follower gate (a connection path exists: [0024] ln 13-19).
40. Regarding claim 102, Rhodes as modified by Han allows for plural transistors, and does not limit the transistors to any particular type (Han: [0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a gate of a global shutter transistor.

41. Regarding claim 103, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said gate of said global shutter transistor (a connection path exists: [0024] ln 13-19).
42. Regarding claim 108, Rhodes discloses (Fig 6-14) a method of forming a CMOS imager (col 8 ln 28-30) comprising the steps of:
 - providing a semiconductor substrate (116+120; col 8 ln 30-32) having a doped layer (120) of a first conductivity type (col 8 ln 32-33);
 - forming a field oxide region (115; col 7 ln 25-28) within said semiconductor substrate;
 - forming a first conductive layer (156) over (no portion is formed under) said field oxide region and said substrate (col 9 ln 49-51);
 - forming an insulating layer (158) over said first conductive layer (col 9 ln 66-67);
 - forming a second conductive layer (160) over said insulating layer (col 10 ln 12-14);
 - patterning said first conductive layer, said insulating layer, and said second conductive layer to form a storage capacitor (col 10 ln 42-45), wherein the entire extent of said storage capacitor is formed wholly over (whole extent formed over; no extent is formed under) and in contact with said field oxide region (since applicant discloses in Fig 10 contact thorough insulating layer 117, Rhodes Fig 5 contact through insulating layer 106 meets the claim limitation).
43. Further regarding claim 108, Rhodes differs from the claimed invention only in not disclosing "patterning...to form a storage capacitor and an electrical element of said

CMOS imager.” Han discloses an analogous CMOS imager [0002] and teaches the method of the current claim ([0015], Fig 4A-4E: [0026] – 0031]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Rhodes by forming the planar capacitor on the same level as the transistor gate, as taught by Han, using the manufacturing method taught by Han; for at least the purpose of reducing the steps of manufacture (Han: [0032]).

44. Regarding claim 109, Rhodes discloses (Fig 8, col 9 ln 8-9, 15-16):

forming a first doped region (155; col 7 ln 61) of a second conductivity type (col 7 ln 30-32) in said doped layer and adjacent said field oxide region (115; col 7 ln 25-27);

forming a second doped region (126) of said second conductivity type in said doped layer spaced from said first doped region (110);

forming a third doped region (130) of said second conductivity type in said doped layer spaced from said second doped region and adjacent said electrical element (128, transfer gate of both Rhodes and Han); and

forming a fourth doped region (134) of said second conductivity type in said doped layer spaced from said third doped region.

45. Regarding claim 110, Rhodes discloses said first conductivity type is p-type (col 7 ln 23-35, col 8 ln 32-34) and said second conductivity type is n-type (col 7 ln 32-33).

46. Regarding claim 111, Rhodes discloses said first doped region, said second doped region, said third doped region, and said fourth doped region are doped at a dopant concentration of from about 1×10^{15} ions/cm² to about 1×10^{16} ions/cm² (col 9 ln 19-23).

47. Regarding claim 112, Rhodes as modified by Han discloses said electrical element is a transistor gate (Han: [0015], Fig 4A-4E: 207; [0026] – 0031]).
48. Regarding claim 113, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said transistor gate (there exists a connection pathway between 235 and 207).
49. Regarding claim 114, Rhodes as modified by Han discloses said electrical element is a reset transistor gate (Han: [0023] ln 17).
50. Regarding claim 115, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said reset transistor gate (a connection path exists: [0024] ln 13-19).
51. Regarding claim 116, Rhodes as modified by Han does not limit the transistor to any particular type (Han: [0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a source follower gate.
52. Regarding claim 117, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said source follower gate (a connection path exists: [0024] ln 13-19).
53. Regarding claim 118, Rhodes as modified by Han does not limit the transistor to any particular type (Han: [0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a row select transistor gate.
54. Regarding claim 119, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said row select transistor gate (a connection path exists: [0024] ln 13-19).

55. Regarding claim 120, Rhodes as modified by Han does not limit the transistor to any particular type (Han: [0024] ln 16-19), therefore, Han's disclosure encompasses all well-known transistor gate types, including a gate of a global shutter transistor.

56. Regarding claim 121, Rhodes as modified by Han discloses (Han: Fig 4E) connecting an electrode of said storage capacitor to said gate of said global shutter transistor (a connection path exists: [0024] ln 13-19).

57. Claims 137-141 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes in view of Luxtermann et al. (US 2001/0015831) – hereinafter Luxtermann.

58. Regarding claim 137, Rhodes discloses (Fig 6-14) a method of forming an imager (col 8 ln 28-30) comprising the steps of:

providing a semiconductor substrate (116+120; col 8 ln 30-32) having a doped layer (120) of a first conductivity type (col 8 ln 32-33);
style="padding-left: 40px;">forming a field oxide region (115; col 7 ln 25-28) in said semiconductor substrate;
style="padding-left: 40px;">forming a photosensor (125; col 7 ln 36-37. Formed: col 8 ln 45 – col 9 ln 25) including a charge collection region (110) of a second conductivity type (col 7 ln 31-32), said charge collection region being provided in said doped layer (col 7 ln 30-31);
style="padding-left: 40px;">forming a floating diffusion region (130; col 7 ln 41-43) for receiving charge from said charge collection region (col 7 ln 61-64); and
style="padding-left: 40px;">connecting an electrode of a {second} charge storage capacitor to said charge collection region by a {second} electrical contact (150; col 7 ln 61-64).

59. Further regarding claim 137, Rhodes differs from the claimed invention in not disclosing plural capacitors; Rhodes does not disclose "connecting an electrode of a first charge storage capacitor to said floating diffusion region by a first electrical contact." Luxtermann discloses an analogous CMOS imager [0001] and teaches (Fig 2B) connecting an additional capacitor (C1) to the floating diffusion region (55). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Rhodes by connecting an additional capacitor to said floating diffusion region (additional capacitor will differ from first only in being formed above and connected to 130 instead of 155), as taught by Luxtermann; for at least the purpose of separating the detection and reading processes (Luxtermann [0006] ln 17-19).

60. Regarding claim 138, Rhodes discloses (Fig 5) said first charge storage capacitor is formed such that the extent of said charge storage capacitor overlies said field oxide region (no portion of 162 lies under 115).

61. Regarding claim 139, Rhodes discloses (Fig 5) a first portion (left side of 162) of said first charge storage capacitor is formed over said field oxide region, and a second portion (right side of 162) of said first charge storage capacitor is formed over an active area of said photosensor (col 8 ln 20-21).

62. Regarding claim 140, Rhodes discloses (Fig 5) said second charge storage capacitor is formed such that the extent of said charge storage capacitor overlies said field oxide region (no portion of 162 lies under 115).

63. Regarding claim 141, Rhodes discloses (Fig 5) a first portion (left side of 162) of said second charge storage capacitor is formed over said field oxide region, and a second portion (right side of 162) of said second charge storage capacitor is formed over an active area of said photosensor (col 8 ln 20-21).

Response to Arguments

64. Applicant's arguments filed 01/10/2006, with respect to the drawings, have been fully considered and are persuasive. The objections to the drawings have been withdrawn.

65. Examiner notes that figures 12 and 14-18 are only circuit diagrams and that structural depictions of "direct contact", "global shutter transistor", and "connected to a gate" have not been provided and therefore remain subject to broadest reasonable interpretation.

66. Applicant has not responded to the rejections under 35 USC § 112, first paragraph made in the office action dated 11/14/2005, however, the "amendment substantially responds to the rejections" and has been entered (MPEP 714.03).

67. The 35 USC § 112, first paragraph rejections of claims 102,103, 120, and 121 have been withdrawn only because applicant's failure to respond to the rejections has been taken as an admission that the recitation "global shutter transistor" does not patentably distinguish over any "transistor".

68. Applicant's arguments filed 01/10/2006, with respect to the claims, have been fully considered but they are not persuasive.

69. Applicant's arguments that:

"capacitor 162 of Rhodes simply does not completely lie over field oxide region 115 so that "the entire extent" of it is "exclusively" or "wholly" located over the field oxide region 115"; and

"In Han, capacitor 230 is formed over both the active area and the isolation region 208, and not "such that the entire extent of said charge storage capacitor overlies exclusively said field oxide region";

are not persuasive. The recitation "exclusively" renders the claims indefinite and is not taken to change the scope of the claims. The recitation "wholly" does not patentably distinguish the claim from Rhodes since the whole capacitor of Rhodes lies over the field oxide region.

70. Applicant's claim language as presented has not been interpreted to mean that the entire extent of said charge storage capacitor lies: within the lateral boundaries of the field oxide region, where lateral means parallel to the substrate; and above the vertical boundaries of the field oxide region, where vertical means perpendicular to the substrate. Additionally, applicant's figure 10 depicts boundaries of the capacitor and field oxide region in only one lateral direction. If applicant amends the claims to indicate that all peripheral lateral boundaries of the capacitor lie inside the peripheral lateral boundaries of the field oxide region, applicant must indicate portions of the originally filed disclosure which provide support for such amendments, see MPEP 706.03(o).

71. Applicant's argument that "In Rhodes, storage capacitor 162...is connected to a fifth doped region 155...and not to the floating diffusion region 130" is not persuasive.

"Floating diffusion region" is interpreted as a diffusion region that is not fixed to a constant potential, and does not patentably distinguish over Rhodes region 155.

72. In response to applicant's arguments against the references individually ("Rhodes is also silent about "connecting an electrode of a first...and...a second charge storage capacitor..." as independent claim 137 recites."), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

73. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case:

regarding the combination of Rhodes and Han, Han teaches an improved method of forming a capacitor in a CMOS imager, and provides the motivation for modification: at least for reducing the steps of manufacture [0032]; and

regarding the combination of Rhodes and Lauxtermann, both references concern CMOS imagers with improved properties, and Lauxterman provides the motivation for modification: at least for separating the detection and reading processes [0006].

Conclusion

74. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

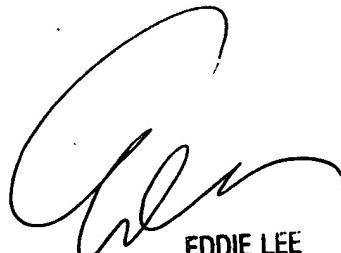
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOA
03/17/2006



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800